DRX-5571

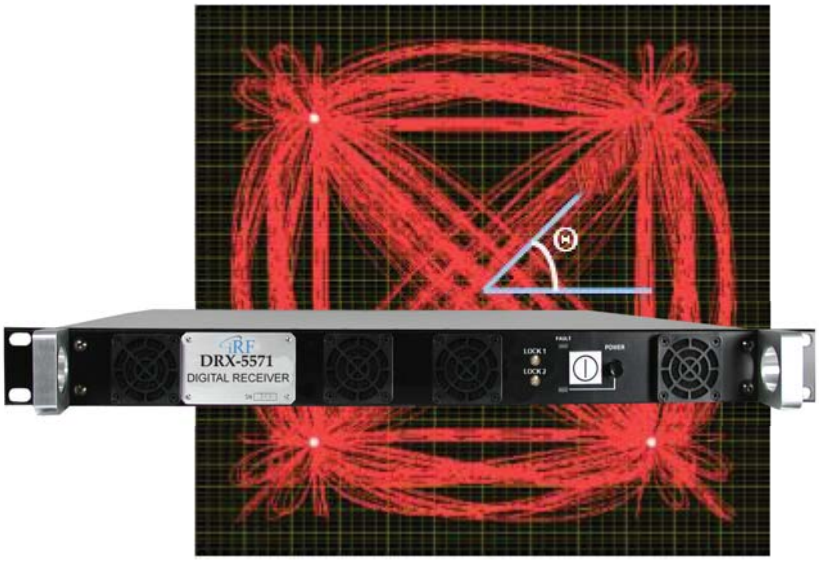
Digital Receiver

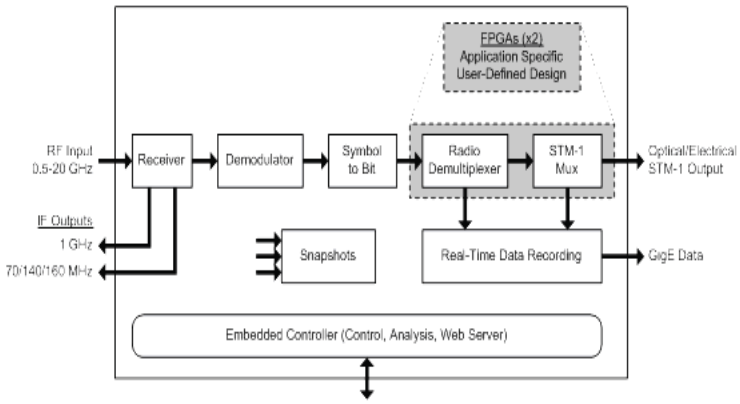
Data Sheet

intelligentRFsolutions

FEATURES

- **Combines microwave tuner, demodulator, and radio demultiplexer in a single integrated 1U unit**
- **Tunes 0.5 to 20 GHz (1 kHz tuning resolution)**
- **Microwave tuner based on field proven SMR-5550i design**
- **Demodulator uses 140 MHz IF up to 57 MHz bandwidth**
- **Demodulates QPSK and 16, 32, & 64-QAM (2 to 46 Mbaud) using field proven demodulator**
- **Includes waveform analysis (auto ID)**
- **Two dedicated FPGAs for radio processing (decoding, descrambling, deframing and demultiplexing)**
- **Includes Development Kit for custom radio demultiplexing designs**
- **STM-1 optical & electrical outputs**
- **Narrowband IF and analog FM video outputs**
- **GUI with Ethernet control interface**





Receiver block diagram

DESCRIPTION

The DRX-5571 is the latest addition to our line of high-performance microwave set-on receivers. The proven RF to IF performance of the SMR-5550 series receivers is combined with FPGA-based demodulation and radio demultiplexing capability. This allows the receiver to fully process microwave signals having complex modulation and encoding schemes down to the underlying radio payload. Thus the DRX-5571 provides a completely integrated system solution for performing capture, analysis, survey, and collection of wideband digital radio RF signals.

Receiver

The DRX-5571 is ideally suited for the reception of signals using QPSK and QAM modulation. Phase noise, group delay, and gain linearity are all optimized to insure maximum fidelity of the IF signal before demodulation. Various analog outputs are provided externally for system flexibility.

Demodulator & Demultiplexer

The tuned 140 MHz analog IF output of the receiver is sent to a flexible FPGA-based demodulator and radio demultiplexer capable of processing up to 64-QAM signals. The radio demultiplexer functionality can be implemented using the included flexible design, or a custom design can be implemented using the provided RLP Development Kit.

Analysis

The DRX-5571 includes a host of analysis software to aid in identification of unknown signals.

An IF spectral plot is available for verification of the input signal. Modulation recognition software is provided to help identify all modulation parameters (type, baud rate, and center frequency)

This equipment does not contain provisions for the installation of an intelligence database (i.e. threat signal parametric data).

This equipment may be subject to U.S. Government export controls. Consult factory for details.

along with automatic configuration of the demodulator for hardware verification.

Radio level processing verification can be accomplished using a library of user pre-defined configurations. The waveform Auto ID software loads each compatible design and analyzes the result. A match is found based on successful overall processing. In addition, a tool is included that provides automatic TCM (trellis coded modulation) identification for demodulated symbols.

The included Trailmapper software provides standard SDH/PDH Mux ID for any system snapshot. A bit raster display (waterfall) has also been provided for viewing and analysis of processed data.

Wideband Demodulator

The DRX-5571 provides flexible wideband demodulation of QPSK and QAM signals for symbol rates up to 46 Mbaud. Signal distortion and interfering impairments are mitigated through filtering, robust timing recovery loops and adaptive equalization.

Radio Level Processing

The DRX-5571 has two large FPGAs dedicated solely to post-demodulator radio level processing (RLP). This provides sufficient resources to demultiplex any complex radio data structure down to the underlying payload for further analysis and processing

RLP solutions can be switched at any time. Specific signal processing setups are stored to and loaded from both the unit and the host as editable text scripts. Four flexible RLP designs are included with the DRX-5571 targeting 2 and 3-level MLCM, TCM, and PDH radios containing various FEC algorithms such as BCH, Reed-Solomon and Viterbi.

Flexible MLCM & TCM RLP Designs

RLP solutions are provided for 2-level MLCM, 3-level MLCM, and TCM radios. See Figure 1. These three designs share a similar processing structure which includes FEC decoding for the specific signal type followed by flexible demultiplexing. The processing blocks such as frame synchronization, descrambling, and deinterleaving can be applied in a flexible order to allow for extraction of the underlying radio payload. Selected portions can then be remultiplexed where necessary for output or recording as a STM-1.

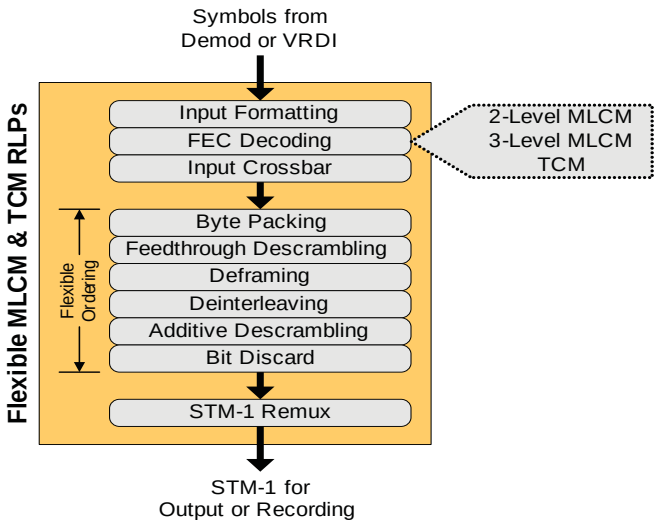


Figure 1

Flexible PDH RLP Design

The PDH RLP design is capable of descrambling, decoding and demultiplexing demodulated symbol streams for a wide range of digital radio formats. Specific implementations are defined by the user in the form of configuration scripts. See Figure 2.

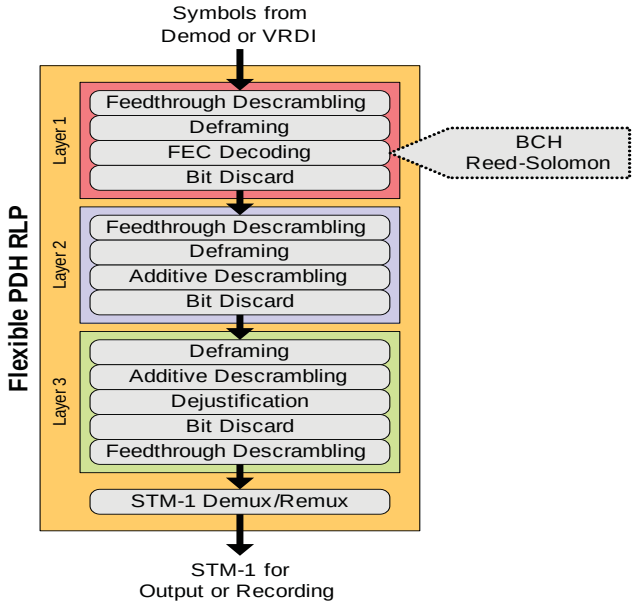


Figure 2

The PDH RLP processor provides three separate levels of frame synchronization supporting multiple rails and tributaries along with FEC decoding (BCH and Reed-Solomon), additive and feedthrough descrambling, and justification processing enabling complex payload extraction. The resulting payload tributaries can be multiplexed up to a STM-1 as appropriate for recording or output.

User-Defined RLP

A Development Kit is also included which, along with the appropriate FPGA vendor tool suite, provides everything necessary to implement custom RLP designs within the two dedicated FPGAs. The Development Kit also provides a custom GUI page for control and status of the user design using a simple text-based description. This provides a custom interface to the radio demultiplexing without requiring any additional software support.

Snapshot

Extensive internal snapshot capability is included to provide access to all levels of data, up to 128 Mbytes at native data rates.

Real-Time Data Recording & Playback

The real-time signal recording capability provides long duration recording direct to the host controller via the dedicated GigE data port. Real-time signal recording supports symbol data (hard and soft-decisions) and any single standard PDH tributary from the resulting STM-1 output (E1, E2, E3, E4 & STM-1).

The data file can also be used for generation of optical and electrical STM-1 outputs using an included PDH remultiplexer for lower-rate tributary data. Post-demodulator symbol data can also be sent to the radio demultiplexing resources on the DRX-5571 for extraction of underlying payload data.

Compact Flash

The DRX-5571 uses removable Compact Flash for storage of FPGA designs, embedded software, and configuration files. This allows the unit to be reconfigured remotely by modifying files on the flash card, or locally by simply changing flash cards. This also allows for quick sanitization of a unit by simply removing the Compact Flash card.

GUI

An intuitive and easy to use GUI is provided that combines the tuner, demodulator, and radio demultiplexer processing in a single interface, along with access to all analysis applications. All flexible processing can be quickly and easily configured, and access to all status is provided including spectrum display, constellation plot, analysis results, and processing status.

DRX-5571 GUI Screen

DRX-5571 RECEIVER SPECIFICATIONS

Frequency coverage	0.5 to 20 GHz
RF input connector	SMA Type
Frequency resolution	1 kHz
Phase noise	0.2° rms, typical
Input VSWR	2.5:1, maximum
Preselection	Suboctave filters
LO radiation	−90 dBm, maximum antenna conducted
Image rejection	60 dB, minimum; 70 dB, typical
Single tone SFDR	53 dB, minimum, 50 MHz BW
1 dB compression (input level)	−15 dBm, typical bypass bandwidth, 30 dB attenuation
Third order input intercept point	−5 dBm, minimum; 0 dBm, typical
LO spurious	−55 dBc, maximum
Tuning speed	150 ms, maximum
1 GHz IF Output	
IF bandwidth (3 dB)	100 MHz, minimum
Gain	20 dB, nominal
Noise Figure	13 dB, maximum, 10 dB, typical
OIP3	+17 dBm, minimum, +24 dBm, typical
Pan IF Output (Fixed Gain)	
Frequency*	70 MHz, 140 MHz
Spectrum sense	Selectable: upright/inverted
IF bandwidth (3 dB)	50 MHz, minimum at 70 MHz 95 MHz, minimum at 140 MHz
Gain	25 dB, nominal
Variable Gain IF Output	
Frequency*	70 MHz, 140 MHz selectable
Noise figure	15 dB, maximum at ≥30 dB gain (at −20 dBm rated output level)
OIP3	+15 dBm, minimum at ≥20 dB gain (at −20 dBm rated output level)
Rated output level	−20 dBm, −15 dBm, −10 dBm, or -5 dBm; user selectable
Absolute gain	+60 dB to −10 dB (at −20 dBm rated output level)
Gain control (MGC)	0 dB to 70 dB of attenuation control in 1 dB steps
Gain control range (AGC)	70 dB, minimum
Bypass/Wideband bandwidths	50 MHz at 70 MHz IF 95 MHz at 140 MHz IF
Standard NBIF filter bandwidths (consult factory for other selections)	140 MHz IF filter BW's: 4, 12, 24, 32, and 48 MHz
Analog demodulator FM video output	
Level (100%)	±0.5 V for Δf = ±1/3 IF BW
Video Response (3 dB)	1/2 Selected IF bandwidth
Coupling	DC
FM Video Gain Range	5% to 100%, 5% steps
Connector Type	BNC, female
Impedance	75 Ω
Digital demodulator	
Modulation types	QPSK, 16-QAM, 32-QAM, 64-QAM
Symbol rates	2 to 46 Mbaud
Equalization	
Feed forward	24-tap, T/2 spaced
Decision feedback	3-tap
Modulation recognition	
Auto-ID	Symbol rate, carrier frequency, modulation type
Types recognized	BPSK, QPSK, SQPSK, 8-PSK, 16 to 256-QAM, FM-FDM, MSK, 2/3/4-FSK

**** 140 MHz IF center frequency must be selected for demodulator to function.***

DRX-5571

RADIO DEMULTIPLEXING SPECIFICATIONS

Included Flexible Radio Demultiplexing Design

Symbol Decoder	
Symbol-to-Bit Mapping	Arbitrary, absolute or differential
Number of Rails	4
Rail Crossbar	Arbitrary
Deframing	
Max Frame Length	32 kbits
Frame Definition	Arbitrary assignment of FAW, overhead, discard, justification control, and FEC parity bits in any combination
FEC Decoding	
Types Supported	Viterbi, Reed-Solomon, & Trellis
Descrambling	
Types supported	Additive feedthrough
Descrambling capabilities	Up to 8 independent rails, 32 taps per rail
Max length of additive pattern	32 Kbits
Additive pattern entry	Polynomial or arbitrary file
Feedthrough pattern entry	Polynomial
Dejustification	
Justification processors	16
Justification control bits	5
Justification control algorithm	Majority rule, positive or negative justification
Snapshot	
Max Length	128 Mbytes

Data Outputs

Optical STM-1	
Data Rate	155.52 Mbps
Power Level	−9.5 to −3 dBm
Wavelength	1270 to 1360 nm, single mode
Connector	LC
Electrical STM-1e	
Data Rate	155.52 Mbps
Encoding	CMI, 1.0 Vp-p nominal
Impedance	50 Ω
Connector	BNC
GigE Data	
Rate	1000 Base-T
Protocol	UDP
Connector	RJ-45

WARRANTY

All intelligentRFsolutions equipment is warranted for one year, except for damage caused by accident or misuse, provided the equipment is returned for repair to the plant in Sparks, Maryland U.S.A

User-Defined Radio Demultiplexing Designs

FPGA	Xilinx Virtex-4 LX100 (x2)
Development environment	Combination of Xilinx tool suite ISE 9.2 or newer (not included) along with included Development Kit that provides all top-level infrastructure required for building an integrated custom FPGA design.

RECEIVER MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Size	1.75” H x 23.16” D x 17” W 4.38 cm H x 58.8 cm D x 43.18 cm W Mounts in Standard 19” rack Note: D dimension is panel to panel and does not include connectors.
Weight	22 lbs. (10.0 kg)
Control interface	10/100Ethernet TCP/IP Configuration via RS-232
Shock	Designed to meet or exceed, MIL-STD-810E, method 516.4, Procedure VI
Vibration	Designed to meet or exceed MIL-STD-810E, method 514.4-1, Category 1
Temperature range, operating	0° to +50°C
Humidity	90% non-condensing at +40° C
AC power	Universal input 100-240 Vac, 50-60 Hz, 130 watts
Built-In-Test (BIT)	Power supply voltages, temperature, phase lock status
EMI shielding	Built to Meet MIL-STD-461C, CE03, and RE02. Tested to EN301 489-01:(2002-08) & EN 301 489-04: (Article 3.1(b) of R&TTE Directive)

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